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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Itsuo Hidaka	:		
Appln. No.: 09/525,802	:	Art Unit:	2815
Filed: March 15, 2000	:	Examiner:	L. Cruz
Title: Semiconductor Device	:	Docket No.	AKM-00301

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Certificate of Mailing

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Bonny Rogers
Name: Bonny Rogers

AMENDMENT AND RESPONSE

Commissioner for Patents
Washington, D.C. 20231

Sir:

This paper is being provided in response to the Final Office Action dated January 3, 2001, for the above-captioned U.S. patent application.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those which may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required for consideration of this paper (including fees for net addition of claims) are authorized to be charged in two originally-executed copies of an Amendment Transmittal Letter filed herewith.

Attached herewith is a set of "clean" rewritten claims as required by 37 C.F.R. § 1.121.

Kindly enter the following amendments:

<u>IN THE CLAIMS:</u>

Please cancel Claims 3, 4, and 17 without prejudice or disclaimer of the subject matter thereof.

Please amend Claims 1-2, 5, 6, 8-10, 13 and 18 as follows:

1. (Thrice Amended) A semiconductor device having multiple wiring layers, comprising:

a signal line which is formed in a wiring layer, and to which a signal voltage is applied;

two adjacent lines which are so adjacent to said signal line as not to be connected thereto, and which are formed in [a] <u>the</u> wiring layer where said signal line is formed;

two intersection lines which are respectively formed in wiring layers, each being present via an insulating layer above or under the wiring layer where said signal line and said adjacent lines are formed, and which are formed along a surface area corresponding to an area which is enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through the insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines and said two intersection lines,

wherein said signal line is completely enclosed by said two adjacent lines, said two intersection lines, and said entire-line-area through-holes, which are one of conductors and semiconductors<u>; and</u>

<u>the electric potentials of said two adjacent lines, said two intersection lines, and said entire-line-area through holes have a same phase as a phase of an electric potential of said signal line</u>.

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2. (Thrice Amended) The semiconductor device according to claim 1, wherein said two adjacent lines are [formed] disposed substantially in parallel to said signal line.

5. (Thrice Amended) A semiconductor device having multiple wiring layers, comprising:

a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate;

a plurality of signal lines which are [formed not] disposed to not intersect each other in [an identical] a same one wiring layer of said multiple wiring layers, and to which signal voltages having a same phase are applied;

two adjacent lines which are [so formed] disposed adjacent [onto] to both sides of said plurality of signal lines as not to be connected thereto, and which are formed in the wiring layer where said plurality of signal lines are formed;

two intersection lines which are formed in a wiring layer each being present via insulating layers above or under the wiring layer where said plurality of signal lines and said two adjacent lines are formed, and which are formed along, a surface area corresponding to an area enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines with said two intersection lines,

wherein said plurality of signal lines are completely enclosed by said two adjacent lines, said two intersection lines, and said plurality of entire-line-area through-holes, which are one of conductors and semiconductors.

6. (Thrice Amended) The semiconductor device according to claim 5, wherein electric potentials of said two adjacent lines, said two intersection lines and said entire-line-area through-holes are retained at a predetermined electric potential value independent of an electric potential applied to said signal line.

8. (Thrice Amended) A semiconductor device having multiple wiring layers, said device comprising:

<u>a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate;</u>

a plurality of signal lines which are formed not to intersect each other in an identical wiring layer, and to which signal voltage having different phases are applied;

two first adjacent lines which are so formed adjacent respectively onto a selected outer two of said plurality of signal lines as not to be connected thereto, and which are formed in the wiring layer where said plurality of signal lines are formed;

at least one second adjacent line which is formed in the wiring layer where said plurality of signal lines are formed, between said plurality of signal lines so as not to be connected to said plurality of signal lines;

two intersection lines, each of which is formed in a wiring layer being present via an insulating layer above or under the wiring layer where said signal lines and said first adjacent lines are formed, and each of which is arranged along a surface area corresponding to an area enclosed by said two first adjacent lines; and

entire-line-area through-holes which respectively penetrate through insulating layers formed between said first and second adjacent lines and said two intersection lines along entire areas of said first and second adjacent lines, and which respectively and electrically connect said first and second adjacent lines with said two intersection lines, wherein said plurality of signal lines are completely enclosed by said two first adjacent lines, said at least one second adjacent line, said two intersection lines, and said entire-line-area through-holes, which are one of semiconductors and conductors.

9. (Thrice Amended) The semiconductor device according to claim 8, wherein electric potentials of said first and second adjacent lines, said two intersection lines and said entire-line-area through-holes are retained at a predetermined electric potential value independent of an electric potential applied to said signal line.

10. (Thrice Amended) A semiconductor device having multiple wiring layers, said device comprising:

a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate;

a plurality of signal lines which are formed substantially in parallel to each other in different wiring layers, and to which signals having a same phase are respectively applied;

a plurality of adjacent lines, each pair of which are so formed adjacent onto both sides of said plurality of signal lines as not to be connected thereto in the wiring layers where said plurality of signal lines are formed;

two intersection lines, each of which is formed in a layer under a lowermost wiring layer where said plurality of signal lines are formed or in a layer above an uppermost wiring layer where said plurality of signal lines are formed, and which are formed along a surface area corresponding to an area enclosed by said plurality of adjacent lines formed on the both extreme sides of said plurality of signal lines;

a plurality of first entire-line-area through-holes which penetrate through an insulating layer arranged between said adjacent lines and said two intersection lines, along entire areas of said adjacent lines, and which electrically connect said adjacent lines with said two intersection lines; and

a plurality of second entire-line-area through-holes which penetrate through an insulating layer arranged between said adjacent lines, along the entire areas of said adjacent lines, and which electrically connects said adjacent lines with each other, wherein said plurality of signal lines are completely enclosed by said adjacent lines, said two intersection lines, said plurality of first entire-line-area through-holes, and said plurality of second entire-line-area through-holes, which are one of conductors and semiconductors.

13. (Thrice Amended) A semiconductor device having multiple wiring layers, said device comprising:

a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate;

a plurality of signal lines which are formed in different wiring layers, and to which signal voltages are respectively applied;

a plurality of adjacent lines, each pair of which are formed either in a lowermost or uppermost wiring layer of the wiring layers where said plurality of signal lines are formed, respectively adjacent onto both sides of a selected one of said plurality of signal lines which is formed in an identical layer, thereby not to be connected to the selected one of said plurality of signal lines;

two first intersection lines, each of which is formed either in a wiring layer under the lowermost wiring layer of said signal lines, or in a wiring layer above the uppermost wiring layer of said signal lines, and each of which is formed along a surface area corresponding to an area enclosed by said pair of adjacent lines formed on the both sides of a corresponding one of said

plurality of signal lines formed either in the lowermost or uppermost wiring layer of said signal lines;

a second intersection line which is formed in a wiring layer formed between said wiring layers of said signal lines, and which is formed along a surface area corresponding to at least one area enclosed by said pair of adjacent lines;

a plurality of first entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said first intersection lines, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said two first intersection lines; and

a plurality of second entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said second intersection line, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said second intersection line,

wherein said plurality of signal lines are completely enclosed by said plurality of adjacent lines, said two first intersection lines, said second intersection line, said plurality of first entire-line-area through-holes, and said plurality of second entire-line-area through-holes, which are one of conductors and semiconductors.

18. (Thrice Amended) A semiconductor device having a structure in which a signal line, to which a signal voltage is applied, is entirely enclosed by one or more conductors or semiconductors, to which a voltage whose electric potential has a same phase as a phase of said signal line is applied, wherein said signal line is completely enclosed by two adjacent lines, two intersection lines, and entire-line-area through-holes, which are one of conductors and semiconductor, said two adjacent lines being adjacent to said signal line and formed in a wiring layer where said signal line is formed, said two intersection lines being formed in a wiring layer above or under the wiring layer wherein said signal line and said adjacent lines are formed, said entire-line-area through-holes penetrating through insulating layers formed between said two adjacent lines and said two intersection lines and said two intersection lines along entire areas of the two adjacent lines;

wherein said semiconductor device includes a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate.

REMARKS

This paper is being provided in response to the January 3, 2001 Final Office Action for the above-referenced application. In this response, Applicant has cancelled Claims 3, 4, and 17, and amended Claims 1, 2, 5, 6, 8-10, 13 and 18 in order to more particularly point out and distinctly claim that which Applicant deems to be the claimed invention. Applicant respectfully submits that the modifications to the claims are all supported by the originally filed application.

The rejection of Claims 1-4 under 35 U.S.C. §102(b) as being anticipated by Landis (U.S Patent No. 4,673,904, hereinafter referred to as "Landis") is hereby traversed and reconsideration

thereof is respectfully requested. Since Claims 3 and 4 have been cancelled herein, the rejection as applied to Claims 3 and 4 is rendered moot. Applicant respectfully submits that Claims 1 and 2, as amended, are patentably distinct over the cited reference.

Independent Claim 1, as amended, recites a semiconductor device having multiple wiring layers. There is a signal line which is formed in a wiring layer, and to which a signal voltage is applied, and two adjacent lines which are so adjacent to the signal line so as not to be connected. The adjacent lines are formed in the wiring layer where the signal line is formed. There are two intersection lines which are respectively formed in wiring layers, each being present via an insulating layer above or under the wiring layer where the signal line and the adjacent lines are formed. The intersection lines are formed along a surface area corresponding to an area which is enclosed by the two adjacent lines. There are a plurality of entire-line-area through-holes which respectively penetrate through the insulating layers formed between the adjacent lines and the two intersection lines, along entire areas of the two adjacent lines, and which electrically connect the two adjacent lines and the two intersection lines. The signal line is completely enclosed by the two adjacent lines, the two intersection lines, and the entire-line-area through-holes, which are made of either conductors or semiconductors. The electric potentials of the two adjacent lines, the two intersection lines, and the entire-line-area through holes have a same phase as a phase of an electric potential of the signal line.

Claim 2 depends from independent Claim 1, and recites further patentable features over the base claim. Dependent claim 2 recites a semiconductor device where the two adjacent lines are substantially parallel to the signal line.

The cited art of Landis discloses a multilayered printed circuit board for supporting and interconnecting the components of an electrical circuit. Landis teaches a method of making a board having a shielded conductor (See Col. 1, Lines 5-10 of Landis' specification). Landis discloses a printed circuit board that includes a metallic base 20 and multiple layers of a plastic dielectric material 78. Imbedded in the dielectric layer are copper foil conductors. The conductors may be completely shielded by tubular shields having a rectangular cross-section, which are formed on the copper base so that they are electrically connected to the ground plane (See Col. 2, Lines 20-31; Figures 2, 3 and 8). For terminating purposes the two extreme portions of each conductor have a vertical section 50 which ends in a square pad flush with the top surface 54 of the printed circuit board, which then are wirebonded to the pads of the IC's 56 and 58 (Col. 2, Lines 32-47).

Applicant respectfully submits that the Landis at least neither discloses nor even suggests a ***semiconductor device***, as set forth in Claim 1. Rather, as pointed out above, Landis discloses conductors having varying degrees of isolation and shielding in which the shielding disclosed uses tubular shields formed on a copper base so that they are electrically connected to the ground plane. There is no disclosure or suggestion in Landis of a semiconductor structure, or of through-holes, or of anything at all having any relation to the present claimed invention.

Landis discloses a tubular shield (40) completely shielding a conductor (26) (See Col. 2, Lines 26). However, Landis discloses nothing about the electric potential of lines or the electric

potential of the shield and neither discloses nor suggests anything about how to deal with these potentials.

The invention of the amended Claim 1 is characterized in that the electrical potential of the shield (two adjacent lines, two intersection lines, and entire-line-area through-holes) has a same phase as that of the electric potential of the signal line. That is, the electric potential of the shield cannot generate noise therefrom affecting the signal line. On the other hand, Landis does not set forth any limitations regarding the electric potential of the shield. Therefore, even if noise from the outside does not occur, the electric potential of the shield may generate noise therefrom affecting the signal of the signal line. The invention of Claim 1 is a novel one different from Landis. Further this invention can solve a problem which is not solvable by Landis. Thus, Claim 1 is also not obvious in view of Landis.

Applicant respectfully disagrees with the suggestion in the Office Action that figure 8 of Landis describes or suggests a semiconductor device, let alone one that contains transistors. That Landis is disclosing only multilayered printed circuit boards and not a semiconductor device may be easily seen by examination of Landis at Col. 1, lines 6, 10, 17 and 46 and Col. 2, lines 8, 20 and 40 where the terms multilayered boards or boards are used. At Col. 1, line 36 the discussion centers on interconnecting electronic components on a board. At Col. 3, line 42 the reference discusses the size of shielded cavity created being around 20 mils by 10 mils in cross section, which for purposes of comparison is 500 microns by 250 microns in cross section. A semiconductor device of the type found in the claimed invention would typically have a shielded region around the signal line with a cross sectional area of around 10 microns by 2 microns.

Thus Applicant respectfully submits that the cited reference does not show, teach, or suggest semiconductor devices.

Therefore, since the cited reference does not contain each and every feature of the claimed invention, the cited reference can not anticipate independent Claim 1 or claims which depend therefrom. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

The rejection of Claims 5 - 18 under 35 U.S.C. §102(b) as being anticipated by Schreiber et al (U.S. Patent No. 4,845,311, hereinafter referred to as "Schreiber") is hereby traversed and reconsideration thereof is respectfully requested. Applicant has cancelled Claim 17 and respectfully submits that the rejection as applied to Claim 17 is rendered moot. Applicant respectfully submits that Claims 5 - 16, and 18, as amended herein, are patentably distinct over the cited reference, for the reasons set forth below.

Independent Claim 5, as amended, recites a semiconductor device having multiple wiring layers including a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate. There is a plurality of signal lines which are disposed to not intersect each other in a same one wiring layer of said multiple wiring_layers, and to which signal voltages having a same phase are applied. Two adjacent lines which are disposed adjacent to both sides of the plurality of signal lines so as not to be connected. The two adjacent lines are formed in the wiring layer where the plurality of signal lines are formed. Two intersection lines are formed in a wiring layer each being present via insulating layers above or under the wiring layer where the plurality of signal lines and said two adjacent lines are formed. They are formed along a surface

area corresponding to an area enclosed by said two adjacent lines. A plurality of entire-line-area through-holes which respectively penetrate through insulating layers formed between the adjacent lines and the two intersection lines, along entire areas of the two adjacent lines, and which respectively and electrically connect the two adjacent lines with the two intersection lines. The plurality of signal lines are completely enclosed by the two adjacent lines, the two intersection lines, and the plurality of entire-line-area through-holes, which are made of conductors or semiconductors. Claims 6 and 7 depend from claim 5.

Independent Claim 8, as amended, recites a semiconductor device having multiple wiring layers, the device includes a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate, a plurality of signal lines which are formed not to intersect each other in an identical wiring layer, and to which signal voltages having different phases are applied. There are two first adjacent lines which are so formed adjacent respectively on a selected outer two of the plurality of signal lines as not to be connected, and which are formed in the wiring layer where the plurality of signal lines are formed. At least one second adjacent line is formed in the wiring layer where the plurality of signal lines are formed, between the plurality of signal lines so as not to be connected to the signal lines. Two intersection lines, each of which is formed in a wiring layer being present via an insulating layer above or under the wiring layer where the signal lines and the first adjacent lines are formed, and each is arranged along a surface area corresponding to an area enclosed by the two first adjacent lines. There are entire-line-area through-holes which respectively penetrate through insulating layers formed between the first and second adjacent lines and the two intersection lines along entire areas of the first and second adjacent lines, and which respectively and electrically connect the first and

second adjacent lines with the two intersection lines. The plurality of signal lines are completely enclosed by the two first adjacent lines, the at least one second adjacent line, the two intersection lines, and the entire-line-area through-holes, which are made of semiconductors or conductors. Claim 9 depends from claim 8.

Independent Claim 10, as amended, recites a semiconductor device having multiple wiring layers including a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate. A plurality of signal lines are formed substantially in parallel to each other in different wiring layers, and to which signals having a same phase are respectively applied. A plurality of adjacent lines, each pair of which are so formed adjacent onto both sides of the plurality of signal lines as not to be connected thereto in the wiring layers where the plurality of signal lines are formed. Two intersection lines, each of which is formed in a layer under a lowermost wiring layer where the plurality of signal lines are formed or in a layer above an uppermost wiring layer where the plurality of signal lines are formed, and which are formed along a surface area corresponding to an area enclosed by the plurality of adjacent lines formed on the both extreme sides of the plurality of signal lines. There are a plurality of first entire-line-area through-holes which penetrate through an insulating layer arranged between the adjacent lines and the two intersection lines, along entire areas of the adjacent lines, and which electrically connect the adjacent lines with the two intersection lines. There is a plurality of second entire-line-area through-holes which penetrate through an insulating layer arranged between the adjacent lines, along the entire areas of the adjacent lines, and which electrically connects the adjacent lines with each other. The plurality of signal lines are completely enclosed by the adjacent lines, the two intersection lines, the plurality of first entire-line-area through-

holes, and the plurality of second entire-line-area through-holes, which are made of conductors or semiconductors. Claims 11 and 12 depend from claim 10.

Independent Claim 13, as amended, recites a semiconductor device having multiple wiring layers including a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate, and a plurality of signal lines which are formed in different wiring layers, and to which signal voltages are respectively applied. There are a plurality of adjacent lines, each pair of which are formed either in a lowermost or uppermost wiring layer of the wiring layers where the plurality of signal lines are formed, and are respectively adjacent on both sides of a selected one of the plurality of signal lines which is formed in an identical layer, but not connected to the selected one of the plurality of signal lines. There are two first intersection lines, each of which is formed either in a wiring layer under the lowermost wiring layer of the signal lines, or in a wiring layer above the uppermost wiring layer of the signal lines, and each of which is formed along a surface area corresponding to an area enclosed by the pair of adjacent lines formed on the both sides of a corresponding one of the plurality of signal lines formed either in the lowermost or uppermost wiring layer of the signal lines. A second intersection line is formed in a wiring layer formed between the wiring layers of the signal lines, and is formed along a surface area corresponding to at least one area enclosed by the pair of adjacent lines. A plurality of first entire-line-area through-holes penetrate through insulating layers respectively formed between the adjacent lines and the first intersection lines, along entire areas of the adjacent lines, and electrically connecting the adjacent lines with the two first intersection lines. A plurality of second entire-line-area through-holes penetrate through insulating layers respectively formed between the adjacent lines and the second intersection line,

along entire areas of the adjacent lines, thereby electrically connecting the adjacent lines with the second intersection line. The plurality of signal lines are completely enclosed by the plurality of adjacent lines, the two first intersection lines, the second intersection line, the plurality of first entire-line-area through-holes, and the plurality of second entire-line-area through-holes, which are made of conductors or semiconductors. Claims 14-16 depend from claim 13.

Independent Claim 18, as amended, recites a semiconductor device having a structure in which a signal line, to which a signal voltage is applied, is entirely enclosed by one or more conductors or semiconductors. A voltage whose electric potential has a same phase as a phase of said signal line is applied. The signal line is completely enclosed by two adjacent lines, two intersection lines, and entire-line-area through-holes, which are made of conductors or semiconductor. The two adjacent lines are adjacent to the signal line and formed in a wiring layer where the signal line is formed. The two intersection lines being formed in a wiring layer above or under the wiring layer where the signal line and adjacent lines are formed. The entire-line-area through-holes penetrating through insulating layers formed between the two adjacent lines and the two intersection lines and the two intersection lines along entire areas of the two adjacent lines. The semiconductor device includes a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate.

The cited art of Schreiber discloses a signal transmission line with flexible coaxial cables capable of transmitting signals in the GHz frequency range without appreciable signal loss and providing high density packaging (See Col. 1, Lines 6-12). The flexible coaxial cables each include a central conducting signal line surrounded by a first dielectric layer. The signal return

line is surrounded by a second dielectric layer which is in turn surrounded by a shield (See Col. 2, Lines 18-34). The shield is made of electrically connected conductor elements. The bottom planar conductor element is electrically connected through a first vertical conductor element to a signal trace. Continuity between a top planar conductor element and the signal trace is established by a second vertical conductor element. The top planar conductor element is electrically connected to the signal trace by a third vertical conductor element. The signal trace is electrically connected to the bottom planar conductor element by a fourth vertical conductor element thereby completing a substantially rectangular shield structure (See Col. 2, Lines 48-61). Each of the shields regions share a common conductor with the neighboring shield, thereby joining together each adjacent coaxial structure (See Col. 2, Line 68-Col. 3, Line 3).

Applicant respectfully submits that the cited reference teaches a flexible cable structure that does not disclose or suggest a semiconductor structure. Applicant further respectfully submits that a coaxial cable is not a transistor or any type of semiconductor device. The fact that the shields share a common wall renders the disclosure appropriate for coaxial cables, but not for semiconductor interconnections.

Applicant further respectfully submits that Schreiber neither discloses nor suggests a ***semiconductor device***, as set forth in the independent Claims. Rather, as discussed above, Schreiber discloses a flexible coaxial cable arrangement that includes a grounded shield structure of electrically connected conductor elements. Schreiber makes no mention or suggestion of internal wiring structure of a semiconductor chip.

Applicant's invention as set forth in Claims 5-16 recites a structure including a plurality of lines to be shielded. The Examiner has pointed out that Schreiber discloses a semiconductor device wherein a plurality of lines, which are shielded, are formed. However, the present invention does not simply include a plurality of lines. The present invention can form a shield which is as small as possible in size in consideration of the position and electric potential of each of the signal lines on the premise that the shield can shield completely so as to prevent a signal of each line from being affected by noise. Schreiber does not consider forming a shield to be small in size in consideration of the position and electric potential of each of the signal lines.

Accordingly, Schreiber neither discloses or suggests at least the above noted feature claimed in Applicants' independent Claim 5, as amended herein. Applicant's independent Claims 8, 10, 13, 17, and 18 are also neither disclosed nor suggested by Schreiber for the same reasons.

The invention of Claim 18 was designed to shield a line completely and to keep the phase of the electrical potential of the shield the same as that of the electric potential of the line. This point is also not disclosed in Schreiber.

In view of the foregoing, Applicant respectfully submits that Schreiber does not anticipate Claims 5-18 since Schreiber does not contain at least the above describe feature , and therefore can not contain each and every feature of the claimed invention. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-951-6676.

Respectfully submitted,
HUTCHINS, WHEELER & DITTMAR

March 20, 2001
Date

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Reg. No. 33,978

Patent Group
Hutchins, Wheeler & Dittmar
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"Clean" Rewritten Claims

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1. A semiconductor device having multiple wiring layers, comprising:

a signal line which is formed in a wiring layer, and to which a signal voltage is applied;

two adjacent lines which are so adjacent to said signal line as not to be connected thereto, and which are formed in the wiring layer where said signal line is formed;

two intersection lines which are respectively formed in wiring layers, each being present via an insulating layer above or under the wiring layer where said signal line and said adjacent lines are formed, and which are formed along a surface area corresponding to an area which is enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through the insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines and said two intersection lines,

wherein said signal line is completely enclosed by said two adjacent lines, said two intersection lines, and said entire-line-area through-holes, which are one of conductors and semiconductors; and the electric potentials of said two adjacent lines, said two intersection lines, and said entire-line-area through holes have a same phase as a phase of an electric potential of said signal line.

2. The semiconductor device according to claim 1, wherein said two adjacent lines are disposed substantially in parallel to said signal line.

3 ~~5~~. A semiconductor device having multiple wiring layers, comprising:

a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate;

a plurality of signal lines which are disposed to not intersect each other in a same one wiring layer of said multiple wiring layers, and to which signal voltages having a same phase are applied;

two adjacent lines which are disposed adjacent to both sides of said plurality of signal lines as not to be connected thereto, and which are formed in the wiring layer where said plurality of signal lines are formed;

two intersection lines which are formed in a wiring layer each being present via insulating layers above or under the wiring layer where said plurality of signal lines and said two adjacent lines are formed, and which are formed along, a surface area corresponding to an area enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines with said two intersection lines,

wherein said plurality of signal lines are completely enclosed by said two adjacent lines, said two intersection lines, and said plurality of entire-line-area through-holes, which are one of conductors and semiconductors.

Cont'd 8 4 ~~6~~. The semiconductor device according to claim 3 ~~5~~, wherein electric potentials of said two adjacent lines, said two intersection lines and said entire-line-area through-holes are retained at a predetermined electric potential value independent of an electric potential applied to said signal line.

6 ~~8~~. A semiconductor device having multiple wiring layers, said device comprising:

a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate;

a plurality of signal lines which are formed not to intersect each other in an identical wiring layer, and to which signal voltage having different phases are applied;

two first adjacent lines which are so formed adjacent respectively onto a selected outer two of said plurality of signal lines as not to be connected thereto, and which are formed in the wiring layer where said plurality of signal lines are formed;

at least one second adjacent line which is formed in the wiring layer where said plurality of signal lines are formed, between said plurality of signal lines so as not to be connected to said plurality of signal lines;

two intersection lines, each of which is formed in a wiring layer being present via an insulating layer above or under the wiring layer where said signal lines and said first adjacent lines are formed, and each of which is arranged along a surface area corresponding to an area enclosed by said two first adjacent lines; and

entire-line-area through-holes which respectively penetrate through insulating layers formed between said first and second adjacent lines and said two intersection lines along entire areas of said first and second adjacent lines, and which respectively and electrically connect said first and second adjacent lines with said two intersection lines, wherein said plurality of signal lines are completely enclosed by said two first adjacent lines, said at least one second adjacent line, said two intersection lines, and said entire-line-area through-holes, which are one of semiconductors and conductors.

3 Cont'd 7 ~~9~~. The semiconductor device according to claim 6 ~~8~~, wherein electric potentials of said first and second adjacent lines, said two intersection lines and said entire-line-area through-holes are retained at a predetermined electric potential value independent of an electric potential applied to said signal line.

8 ~~10~~. A semiconductor device having multiple wiring layers, said device comprising:

a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate;

a plurality of signal lines which are formed substantially in parallel to each other in different wiring layers, and to which signals having a same phase are respectively applied;

a plurality of adjacent lines, each pair of which are so formed adjacent onto both sides of said plurality of signal lines as not to be connected thereto in the wiring layers where said plurality of signal lines are formed;

two intersection lines, each of which is formed in a layer under a lowermost wiring layer where said plurality of signal lines are formed or in a layer above an uppermost wiring layer where said plurality of signal lines are formed, and which are formed along a surface area corresponding to an area enclosed by said plurality of adjacent lines formed on the both extreme sides of said plurality of signal lines;

a plurality of first entire-line-area through-holes which penetrate through an insulating layer arranged between said adjacent lines and said two intersection lines, along entire areas of said adjacent lines, and which electrically connect said adjacent lines with said two intersection lines; and

a plurality of second entire-line-area through-holes which penetrate through an insulating layer arranged between said adjacent lines, along the entire areas of said adjacent lines, and which electrically connects said adjacent lines with each other, wherein said plurality of signal lines are completely enclosed by said adjacent lines, said two intersection lines, said plurality of first entire-line-area through-holes, and said plurality of second entire-line-area through-holes, which are one of conductors and semiconductors.

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11 ~~13~~. A semiconductor device having multiple wiring layers, said device comprising:

a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate;

a plurality of signal lines which are formed in different wiring layers, and to which signal voltages are respectively applied;

a plurality of adjacent lines, each pair of which are formed either in a lowermost or uppermost wiring layer of the wiring layers where said plurality of signal lines are formed, respectively adjacent onto both sides of a selected one of said plurality of signal lines which is formed in an identical layer, thereby not to be connected to the selected one of said plurality of signal lines;

two first intersection lines, each of which is formed either in a wiring layer under the lowermost wiring layer of said signal lines, or in a wiring layer above the uppermost wiring layer of said signal lines, and each of which is formed along a surface area corresponding to an area enclosed by said pair of adjacent lines formed on the both sides of a corresponding one of said plurality of signal lines formed either in the lowermost or uppermost wiring layer of said signal lines;

a second intersection line which is formed in a wiring layer formed between said wiring layers of said signal lines, and which is formed along a surface area corresponding to at least one area enclosed by said pair of adjacent lines;

a plurality of first entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said first intersection lines, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said two first intersection lines; and

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a plurality of second entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said second intersection line, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said second intersection line,

wherein said plurality of signal lines are completely enclosed by said plurality of adjacent lines, said two first intersection lines, said second intersection line, said plurality of first entire-line-area through-holes, and said plurality of second entire-line-area through-holes, which are one of conductors and semiconductors.

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15 ~~18~~. (Thrice Amended) A semiconductor device having a structure in which a signal line, to which a signal voltage is applied, is entirely enclosed by one or more conductors or semiconductors, to which a voltage whose electric potential has a same phase as a phase of said signal line is applied, wherein said signal line is completely enclosed by two adjacent lines, two intersection lines, and entire-line-area through-holes, which are one of conductors and semiconductor, said two adjacent lines being adjacent to said signal line and formed in a wiring layer where said signal line is formed, said two intersection lines being formed in a wiring layer above or under the wiring layer wherein said signal line and said adjacent lines are formed, said entire-line-area through-holes penetrating through insulating layers formed between said two adjacent lines and said two intersection lines and said two intersection lines along entire areas of the two adjacent lines;

wherein said semiconductor device includes a plurality of transistors and passive semiconductor devices disposed upon a semiconductor substrate.